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10/632,772	08/01/2003	Gregg Bernard Lesartr	200209214-1	3656

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EXAMINER	
WAI, ERIC CHARLES	

ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

mw

Office Action Summary	Application No.	Applicant(s)	
	10/632,772	LESARTR ET AL.	
	Examiner	Art Unit	
	Eric C. Wai	2195	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 July 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-8,12-14,16,17 and 21-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-8,12-14,16,17 and 21-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 August 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1, 3-8, 12-14, 16-17, and 21-31 are presented for examination.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the step of claim 27 wherein the logic is configured to refrain from purging the instruction queue in response to the purge signal must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner,

the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

3. Claims 3 and 5 objected to because of the following informalities: Improperly dependent from cancelled claim 2. For purposes of examination, they will be interpreted to depend off claim 1. Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claim 27 is rejected under 35 U.S.C. 112, first paragraph, as based on a disclosure which is not enabling. The logic configured to refrain from purging the instruction queue is critical or essential to the practice of the invention, but included in the claim(s) is not enabled by the disclosure. See *In re Mayhew*, 527 F.2d 1229, 188 USPQ 356 (CCPA 1976).

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 22 and 30 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

a. The following terms lack antecedent basis in the claims:

i. Claim 22, "the instruction".

ii. Claim 30, "the instruction queue".

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1, 3-4, 12, 16-17, and 21-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (AAPA) in view of Moore et al. (US Pat No. 5,437,017 hereinafter Moore).

10. Regarding claim 1, AAPA teaches a processor purging system, comprising:

a translation lookaside buffer (TLB) having a plurality of translation pairs ([0001] lines 2-4);

at least one memory cache ([0001] line 2); and

logic configured to make a determination whether at least one of the translation pairs corresponds to a purge signal and to purge, in response to the purge signal, each of the translation pairs in the TLB corresponding to the purge signal ([0005] lines 5-7, wherein logic inherently must be capable of detecting whether a translation pair corresponds to the signal).

11. AAPA does not explicitly teach that the logic further configured to transmit, based on the determination, a purge detection signal indicative of whether at least one translation pair in the TLB corresponds to the purge signal and to determine, based upon the purge detection signal, whether to search the memory cache for a information to be purged based on the purge signal

12. Moore teaches a system and method for maintaining TLB coherency between the TLB and memory queues (i.e. instruction queue) in a multiprocessor system (abstract). Moore accomplishes this by broadcasting a TLB invalidate instruction to all processors (Fig 4). Once all processors have indicated that the instruction has completed execution, a determination is made whether the memory queue has reached coherency (col 9 lines 30-42).

13. It would have been obvious to one of ordinary skill in the art at the time of the invention to include transmitting a signal to indicate when to check for coherency in the memory queue as taught by Moore. One would be motivated by the desire to ensure that the TLB was purged of all invalid entries before performing a coherency check on the rest of the memory queues.

14. AAPA and Moore differ from the claimed invention by not teaching transmitting a purge detection signal indicative of whether at least one translation pair in the TLB corresponds to the purge signal. However it would have been obvious to one of ordinary skill in the art at the time of the invention to perform the coherency check as taught by Moore only when such a check is necessary. One would be motivated by the desire to increase the efficiency of the system by reducing unnecessary actions.

15. Regarding claim 3, AAPA teaches that the memory cache further comprises an instruction queue ([0005] lines 7-8).

16. Regarding claim 4, AAPA teaches that the memory cache further comprises a mini-TLB ([0005] lines 7-8).

17. Regarding claims 12, 16-17 and 24, they are the method claims of claim 1 above. Therefore, they are rejected for the same reasons as claim 1 above.

18. Regarding claim 21, Moore teaches wherein the logic is further configured to determine whether to purge the instruction queue based on the purge detection signal (Fig 5, wherein step 124 is only executed after the TLBI instruction has been executed by all processors).

19. Regarding claim 22, AAPA and Moore do not teach the step of purging the instruction if the purge detection signal indicates that at least one of the translation pairs in the TLB corresponds to the purge signal.

20. It would have been obvious to one of ordinary skill in the art at the time of the invention to purge an instruction should the instruction refer to invalid addresses within the TLB.

21. Regarding claim 23, AAPA and Moore do not explicitly teach that the determining step comprises the step of determining not to purge the instruction queue in response to the purge signal if none of the translation pairs correspond to the purge signal.

22. It would have been obvious to one of ordinary skill in the art at the time of the invention to not purge the instruction queue if such action was unnecessary. One would be motivated by the desire to increase the efficiency of the system.

23. Regarding claims 25-26, they are the processor claims of claim 1 above. Therefore, they are rejected for the same reasons as claim 1 above.

24. Regarding claim 27, Moore teaches that the logic is configured to refrain from purging the instruction queue in response to the purge signal if at least one of the translation pairs stored in the TLB corresponds to the purge signal (col 9 lines 9-42, wherein the purging of the instruction queue occurs only after all processors have performed the TLBI instruction).

25. Regarding claims 28-31, they are the method claims of claim 1 and 3 above. Therefore, they are rejected for the same reasons as claim 1 and 3 above.

26. Claims 5-8, and 13-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA and Moore, in view of Matthews et al. (US Pat No. 6,560,689 hereinafter Matthews).

27. Regarding claim 5, AAPA and Moore do not explicitly teach compare logic configured to compare the purge signal with each of the plurality of translation pairs and to transmit a plurality of match signals corresponding respectively to the plurality of translation pairs, each of the match signals indicating whether the corresponding translation pair corresponds to the purge signal.

28. Matthews teaches setting Purge Enable bits of the TLB entries when those entries match to a virtual address to be purged (col 7 lines 1-27). It would have been obvious to one of ordinary skill in the art at the time of the invention to include setting a match signal to each translation pair that corresponds to the purge signal. One would be motivated by the desire to indicate which entries should be purged.

29. Regarding claim 6, Matthews teaches that the logic is further configured to collapse the match signals into the purge detection signal (col 7 lines 1-2, wherein the input virtual address is compared against all CAM entries to generate match signals).

30. Regarding claims 7-8, Matthews does not explicitly teach that the logic comprises a plurality of tiered logical AND or OR gates configured to collapse the match signals into the purge detection signal.

31. It would have been obvious to one of ordinary skill in the art to use logical AND and OR gates to collapse a plurality of signals together. It is well known in the art that AND and OR gates are the building blocks of logical circuits.

32. Regarding claims 13-14, they are the method claims of claims 5-6 above. Therefore, they are rejected for the same reasons as claims 5-6 above.

Response to Arguments

33. Applicant's arguments with respect to claim 1 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

34. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

35. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric C. Wai whose telephone number is 571-270-1012. The examiner can normally be reached on Mon-Thurs, 9am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng - Ai An can be reached on 571-272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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